UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,485	04/09/2004	Lawrence A. Booth JR.	42P19129	1216

8791 7590 02/07/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,485	BOOTH, LAWRENCE A.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 6-7, filed November 21, 2005, with respect to the rejection(s) of claim(s) 1-22 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Naughton (US005519825A).

3. With regard to Claims, Applicant argues that as Beitel's (US005150312A) buffer B is not a final storage area of display data and does not hold the display data readily for display, buffer B cannot possibly teach or suggest the frame buffer as claimed (pages 6-7).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Naughton.

4. Applicant's arguments, filed November 21, 2005, with respect to Claims 2, 9-12, and 15, have been fully considered but they are not persuasive.

5. With regard to Claim 2, Applicant argues that nothing in Beitel indicates that copying display data into buffer B occurs simultaneously with reading the display data from display (screen) memory 1 (pages 7-8).

In reply, the Examiner disagrees. Beitel describes that copying display data into buffer B occurs simultaneously with reading the display data from display (screen) memory 1 (*this movement occurs without generating screen flicker in that writing the buffer B image to the screen memory 1 causes the object to be totally erased from the region 10a while simultaneously being written to the region 10b*, Col. 4, lines 26-34).

6. With regard to Claims 9-12 and 15, Applicant argues that Beitel discloses that buffer B is located in main memory 4, which cannot possibly be placed on the limited space of a graphic chip (page 8).

In reply, the Examiner disagrees. Beitel does not mention the size of buffer B, and therefore buffer B could be placed on a graphics chip.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-11, 13, 14, and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beitel (US005150312A) in view of Naughton (US005519825A), further in view of Cross (US006108015A).

10. With regard to Claim 1, Beitel describes an apparatus comprising a CPU (2, Figure 1) that controls the display (10) (Col. 2, lines 43-47). Buffer B is coupled to the CPU (Col. 2, lines 40-43; Col. 3, lines 52-54). Display data is copied from the display memory (1) to frame buffer A (Col. 2, line 68-Col. 3, line 2), and then from buffer A to buffer B (Col. 3, lines 62-64; Col. 1, lines 57-62), wherein the display data copied into buffer B is the same display data read by the CPU from the display memory (Col. 2, lines 43-47; Col. 2, line 60-Col. 3, line 2). Control circuitry is inherently included to perform the copying.

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes an apparatus comprising a CPU (108, Figure 1) that controls the display (118). The back frame buffer (112) is coupled to the CPU (Col. 6, lines 39-42). The display displays the first frame from the front frame buffer (114) (Col. 3, lines 9-12). All sprite objects that have not moved from the first frame are copied into the back frame buffer (Col. 3, lines 16-21).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Beitel so that buffer B is a frame buffer as suggested by Naughton because Naughton suggests the advantage of being able to directly read the data from the frame buffers to the display (Col. 3, lines 9-21) instead of going through buffer A, buffer B, and the display memory as taught in Beitel.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Beitel and Naughton to include a display controller as suggested by Cross because Cross suggests that a display controller is the "master" for the specific application of display and thus frees up the CPU to perform computational tasks. Moreover, the architecture of a display controller optimizes it to perform graphics and video functions in a manner superior to that of a general purpose microprocessor (Col. 4, line 65-Col. 5, line 4). It would be obvious to provide both an internal frame buffer and an external frame buffer as suggested by Cross because Cross suggests that an on-chip memory provides the controller with fast access storage, and the off-chip memory allows the controller to interface with a memory which may be substantially larger than that which can be provided on-chip (Col. 2, lines 40-48).

11. With regard to Claim 2, Beitel describes that when the display data is copied into buffer B, the present image of the object that was in buffer B is erased (Col. 3, lines 62-68). The first image disappears from the present portion of the second image while simultaneously appearing within the next portion of the second image, thereby avoiding display screen flicker (Col. 1, lines 63-68). Therefore, the display data is copied into frame buffer B simultaneously with the CPU (2, Figure 1) containing the display controller (Col. 2, lines 43-47) reading the display data from the display memory (1). Beitel describes that copying display data into buffer B occurs simultaneously with reading the display data from display (screen) memory 1 (*this movement occurs without generating screen flicker in that writing the buffer B image to the screen memory 1 causes the object to be totally erased from the region 10a while simultaneously being written to the region 10b*, Col. 4, lines 26-34).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

12. With regard to Claim 3, Beitel describes determining if the object is to continue to move across the display screen (28, Figure 3; Col. 4, lines 35-36). If further movement is desired, new display data from buffer A (22, 32) which is from display memory (1, Figure 1; Col. 4, lines 1-5) is copied into buffer B (20, Figure 3, Col. 4, lines 37-47). Therefore, the CPU (2, Figure 1)

containing the display controller (Col. 2, lines 43-47) reads the display data from buffer B (26, Figure 3; Col. 4, lines 19-22) until the CPU receives a signal indicating that buffer A contains the most recent display data from display memory (28; Col. 4, lines 35-36; Col. 4, lines 1-5), then the new display data (22, 32) is copied into buffer B (20; Col. 4, lines 27-47).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

13. With regard to Claim 4, Beitel describes that the CPU reads the display data from buffer B at least one time after a new frame display refresh operation (Col. 4, lines 31-34).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

14. With regard to Claim 5, Beitel does not teach that the display controller, the internal frame buffer and the control circuitry are disposed on a single graphics chip and the external

frame buffer is disposed on another chip separate from the graphics chip. However, Cross describes that the display controller (103, Figure 1), the internal frame buffer (104a) and the control circuitry are disposed on a single graphics chip (107) (Col. 4, lines 44-46) and the external frame buffer (104b) is disposed on another chip separate from the graphics chip (Col. 4, lines 40-44).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Beitel so that the display controller, the internal frame buffer and the control circuitry are disposed on a single graphics chip and the external frame buffer is disposed on another chip separate from the graphics chip as suggested by Cross because Cross suggests the advantage of substantially reducing the capacitive and inductive loading between the display controller and the internal frame buffer in the absence of chip to chip interconnections (Col. 5, lines 50-54). The advantages of the external memory were discussed in the rejection for Claim 1.

15. With regard to Claim 6, Beitel does not teach that the display controller, the internal frame buffer and the control circuitry are disposed on a single processor chip. However, Cross describes that the display controller (103, Figure 1), the internal frame buffer (104a) and the control circuitry are disposed on a single processor chip (107) (Col. 4, lines 44-46), as discussed in the rejection for Claim 5.

16. With regard to Claim 7, Beitel does not teach that the control circuitry comprises at least one register to hold at least one data transaction of display data. However, Cross describes that

the control circuitry comprises at least one register (201-203, Figure 2) to hold at least one data transaction of display data (Col. 2, lines 49-51; Col. 5, lines 34-38).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Beitel so that the control circuitry comprises at least one register to hold at least one data transaction of display data as suggested by Cross because Cross suggests that registers help to eliminate complex timing schemes (Col. 2, lines 49-51).

17. With regard to Claim 8, Beitel does not teach that the control circuitry is to generate a write signal to be used by the internal frame buffer based on an external memory read signal and a memory clock signal. However, Cross describes that the control circuitry is to generate a write signal to be used by the internal frame buffer (104a, Figure 1) based on an external memory (104b) read signal and a memory clock signal (Col. 6, lines 11-25; Col. 9, lines 16-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Beitel so that the control circuitry is to generate a write signal to be used by the internal frame buffer based on an external memory read signal and a memory clock signal as suggested by Cross because Cross suggests that the data is alternatedly received from the memories (Col. 5, lines 34-41), and therefore the timing of the memories must depend on each other.

18. With regard to Claim 9, Beitel describes a system comprising a processor (2, Figure 1; Col. 2, lines 43-47) and a display device (10; Col. 2, lines 32-33). The CPU controls the display (10) (Col. 2, lines 43-47). Buffer B is coupled to the CPU (Col. 2, lines 40-43; Col. 3, lines 52-

54). Display data is copied from the display memory (1) to buffer A (Col. 2, line 68-Col. 3, line 2), and then from buffer A to buffer B (Col. 3, lines 62-64; Col. 1, lines 57-62), wherein the display data copied into buffer B is the same display data read by the CPU from the display memory (Col. 2, lines 43-47; Col. 2, line 60-Col. 3, line 2). Data copy circuitry is inherently included to perform the copying. This copying occurs during a new frame display refresh operation (Col. 4, lines 31-34). Beitel describes determining if the object is to continue to move across the display screen (28, Figure 3; Col. 4, lines 35-36). If further movement is desired, new display data from buffer A (22, 32) which is from display memory (Col. 4, lines 1-5) is copied into buffer B (20, Figure 3, Col. 4, lines 37-47). Therefore, subsequent display refresh operations are accomplished by the CPU (Col. 2, lines 19-22) retrieving data from buffer B (26, Figure 3; Col. 4, lines 19-22) until a new frame is available in display memory (28; Col. 4, lines 35-36), then the new display data (22, 32; Col. 4, lines 1-5) is copied into buffer B (20; Col. 4, lines 27-47).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal memory array, and the display controller, internal memory array and data copy circuitry are all on one graphics chip. However, Cross describes a system (100, Figure 1) comprising a processor (101); a display device (106) (Col. 4, lines 37-40); a graphics chip (107) coupled between the processor and the display device, the graphics chip including a display controller (103), an internal memory array (104a) and control circuitry (Col. 4, lines 43-46); and an external memory array (104b) disposed on another chip separate from the graphics chip (Col. 4,

line 43), wherein the control circuitry is coupled between the external memory array and the internal memory array (Col. 5, lines 25-30). This would be obvious for the same reasons given in the rejections for Claims 1 and 5.

19. With regard to Claim 10, Claim 10 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

20. With regard to Claim 11, Beitel describes that the display data copied into the first memory array (buffer B) is the same display read by the CPU from the other memory array (display memory 1, Figure 1), as discussed in the rejection for Claim 1.

However, Beitel does not teach a display controller and that the first memory array is an internal memory array. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal memory array (104a) and an external memory array (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

21. With regard to Claim 13, Claim 13 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

22. With regard to Claim 14, Claim 14 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

23. With regard to Claim 16, Beitel describes a method comprising reading display data from display memory (1, Figure 1) into buffer A (Col. 3, line 68-Col. 3, line 2), and from buffer A into buffer B (Col. 3, lines 62-64) by a CPU (2) (Col. 2, lines 43-47) during a new frame display refresh operation (Col. 4, lines 31-34); and loading a copy of the display data from display memory to buffer A (Col. 3, line 68-Col. 3, line 2), and from buffer A to buffer B (Col. 3, lines 62-64; Col. 1, lines 57-62) during the new frame display refresh operation (Col. 4, lines 31-34).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

24. With regard to Claim 17, Beitel describes determining if the object is to continue to move across the display screen (28, Figure 3; Col. 4, lines 35-36). If not the method halts (30; Col. 4, lines 36-37), and therefore the same display will remain on the display screen, and therefore the same display data in buffer B will inherently continue to be read (26, Col. 4, lines 19-22). Therefore, Beitel discloses determining if a new frame is available in the display memory (28, Col. 4, lines 35-36); and reading the display data in buffer B by the CPU (Col. 2, lines 43-47) during subsequent display refresh operations if a new frame is not available in display memory (26, Col. 4, lines 19-22).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

25. With regard to Claim 18, Beitel describes that the display data from the external frame buffer (1, Figure 1) includes rendered graphics objects or an entire frame (Col. 2, line 67-Col. 3, line 2).

26. With regard to Claim 19, Claim 19 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

27. With regard to Claim 20, Beitel discloses that the loading of the data from the display memory (1, Figure 1) to buffer A (Col. 2, line 67-Col. 3, line 2), and from buffer A to buffer B (Col. 3, lines 62-64; Col. 1, lines 57-62) is inherently accomplished using data copy circuitry.

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach that buffer B is an internal frame buffer. However, Cross describes an apparatus comprising a display controller (103, Figure 1); an

internal frame buffer (104a) and an external frame buffer (104b) coupled to the display controller (Col. 4, lines 35-46), as discussed in the rejection for Claim 1.

28. With regard to Claim 21, Claim 21 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

29. With regard to Claim 22, Beitel describes loading data from the display memory (1, Figure 1) to buffer A (Col. 2, line 67-Col. 3, line 2), and from buffer A to buffer B (Col. 3, lines 62-64; Col. 1, lines 57-62).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach that the buffer B is an internal frame buffer, and temporarily storing at least one data transaction of the display data in a register; and writing the stored data into the internal frame buffer based on an external memory read signal. However, Cross describes an internal frame buffer (104a, Figure 1, Col. 4, lines 40-43), and temporarily storing at least one data transaction of the display data in a register (201-203, Figure 2; Col. 2, lines 49-51; Col. 5, lines 34-38); and writing the stored data into the internal frame buffer (104a) based on an external memory read signal (Col. 6, lines 11-25; Col. 9, lines 16-19). This would be obvious for the same reasons given in the rejections for Claims 7 and 8.

30. Claims 9-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beitel (US005150312A) in view of Naughton (US005519825A), further in view of Aleksic (US 20040150647A1).

31. With regard to Claim 9, Beitel describes a system comprising a processor (2, Figure 1; Col. 2, lines 43-47) and a display device (10; Col. 2, lines 32-33). The CPU controls the display (10) (Col. 2, lines 43-47). Buffer B is coupled to the CPU (Col. 2, lines 40-43; Col. 3, lines 52-54). Display data is copied from the display memory (1) to buffer A (Col. 2, line 68-Col. 3, line 2), and then from buffer A to buffer B (Col. 3, lines 62-64; Col. 1, lines 57-62), wherein the display data copied into buffer B is the same display data read by the CPU from the display memory (Col. 2, lines 43-47; Col. 2, line 60-Col. 3, line 2). Data copy circuitry is inherently included to perform the copying. This copying occurs during a new frame display refresh operation (Col. 4, lines 31-34). Beitel describes determining if the object is to continue to move across the display screen (28, Figure 3; Col. 4, lines 35-36). If further movement is desired, new display data from buffer A (22, 32) which is from display memory (Col. 4, lines 1-5) is copied into buffer B (20, Figure 3, Col. 4, lines 37-47). Therefore, subsequent display refresh operations are accomplished by the CPU (Col. 2, lines 19-22) retrieving data from buffer B (26, Figure 3; Col. 4, lines 19-22) until a new frame is available in display memory (28; Col. 4, lines 35-36), then the new display data (22, 32; Col. 4, lines 1-5) is copied into buffer B (20; Col. 4, lines 27-47).

However, Beitel does not teach that buffer B is a frame buffer. However, Naughton describes that the back buffer is a frame buffer, as discussed in the rejection for Claim 1.

However, Beitel and Naughton do not teach a display controller and that buffer B is an internal memory array, and the display controller, internal memory array and data copy circuitry are all on one graphics chip. However, Aleksic describes a display controller (330, Figure 3) and an internal memory array (360) [0021], and the display controller, internal memory array and control circuitry (350) are all on one graphics chip (118; *graphics system 118 includes an LCD controller 330, a memory controller 350, and embedded memory 360*, [0021], *components of the graphics system 118 are formed on a common semiconductor*, [0018], lines 18-21).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Beitel and Naughton to include a display controller as suggested by Aleksic because Aleksic suggests that a display controller is needed to identify appropriate signals to power the display device to represent the rendered image data [0022]. It would be obvious to provide both an internal memory array and an external memory array as suggested by Aleksic because Aleksic suggests that external memory requires additional power for accessing data ([0018], lines 25-30), so internal memory is needed to reduce power usage, but external memory is also needed because the amount of rendered image data to be stored is generally larger than the size of memory available internal to the graphics system ([0018], lines 15-18). It would be obvious to have the display controller, internal memory array and control circuitry all on one graphics chip as suggested by Aleksic because Aleksic suggests that accessing components outside of a graphics chip requires additional power for accessing data ([0018], lines 25-30), so having the components on one graphics chip saves power.

32. With regard to Claim 10, Beitel describes that when the display data is copied into buffer B, the present image of the object that was in buffer B is erased (Col. 3, lines 62-68). The first image disappears from the present portion of the second image while simultaneously appearing within the next portion of the second image, thereby avoiding display screen flicker (Col. 1, lines 63-68). Therefore, the CPU (Col. 2, lines 43-47) retrieves the data from the display memory (1) simultaneously with copy of the data from the display memory to buffer A, and from buffer A to buffer B (Col. 2, line 68-Col. 3, line 2; Col. 3, lines 62-68; Col. 1, lines 63-68).

However, Beitel does not teach a display controller and that frame buffer B is an internal memory array. However, Aleksic describes a display controller (330, Figure 3) and an internal memory array (360) [0021], as discussed in the rejection for Claim 9.

33. With regard to Claim 11, Beitel describes that the display data copied into the first memory array (buffer B) is the same display read by the CPU from the other memory array (display memory 1, Figure 1), as discussed in the rejection for Claim 1.

However, Beitel does not teach a display controller and that the first memory array is an internal memory array. However, Aleksic describes a display controller (330, Figure 3) and an internal memory array (360) [0021], as discussed in the rejection for Claim 9.

34. With regard to Claim 12, Beitel does not teach that a graphics generator is disposed on the graphics chip. However, Aleksic describes that a graphics generator (310, Figure 3) is disposed on the graphics chip (118; graphics system 118 includes a graphics engine 310, [0021-

0022] components of the graphics system 118 are formed on a common semiconductor, [0018], lines 18-21).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Beitel so that as a graphics generator is disposed on the graphics chip suggested by Aleksic because Aleksic suggests that a graphics generator is needed to process graphics commands such as bitblt, scaling, object rotation, alpha blending, and anti-aliasing commands [0022], and it would be advantageous to have to the graphics generator on the graphics chip to save power, because accessing components outside of the graphics chip requires additional power ([0018], lines 25-30).

35. With regard to Claim 15, Beitel describes two memory arrays and the data copy circuitry, as discussed in the rejection for Claim 1.

However, Beitel does not teach a display controller and an internal memory array, and a portable power source coupled to power the display controller, the internal memory array, the external memory array and the data copy circuitry. However, Aleksic describes a display controller (330, Figure 3) and an internal memory array (360) [0021], and a portable power source (125, Figure 2, [0015]) coupled to power the display controller, the internal memory array, the external memory array (119) (*memory 119 is external to graphics system 118*, [0018], lines 7-10) and the control circuitry (350, Figure 3) [0021, 0015].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Beitel to include a portable power source coupled to power the display controller, the internal memory array, the external memory array and the data copy

circuitry as suggested by Aleksic because Aleksic suggests that portable power sources are needed for many handheld devices, such as personal digital assistants and mobile phones [0003-0004]. It would be obvious to include a display controller and an internal memory array for the same reasons given in the rejection for Claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner